REMARKS

In the Office Action dated August 27, 2003, claims 21-40 are pending and claims 21-40 stand rejected. In this response, claims 21, 30, and 39-40 have been amended. Portions of the specification have been amended to correct some clerical errors. No new matter has been added. Reconsideration of this application as amended is respectfully requested.

Claims 21-40 are provisionally rejected under judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-31 of copending Application No. 09/023,172 and claims 18-30 of copending Application No. 09/023,234. Since this is a provisional rejection, applicant submits that a terminal disclaimer will be submitted when the present application is allowed.

Claims 21, 23, 30, and 39-40 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,357,621 of Cox ("Cox"). In view of foregoing amendment, applicant submits that claims 21-40 are not anticipated by Cox. Specifically, independent claim 21 includes a memory module controller that servers as an interface between one or more memory devices of the memory module and a system memory controller and the system memory bus. The memory module controller separates the one or more memory devices from the system memory controller and the memory bus, such that the memory devices of different memory modules and the system memory bus can operate in different operating environments, such as, for example, different design specifications from different vendors, different signaling protocols even if they are incompatible with each other (as claimed in claims 39-40), different power supplied voltages (as claimed in claims 28 and 34), and different frequencies of clock signals (as claimed in claim 29), etc., which lead to efficient power management of

the memory devices (as claimed in claims 23-27). Applicant submits that the above limitations are absent from Cox.

Rather, Cox discloses a conventional memory module 20 that the memory devices or arrays (e.g., memory BLKs 1 and 2) are directly coupled to the system memory bus and controlled by the MCL system controller 11. See, for example, Fig. 1 of Cox. The alleged memory module controller (including control logic 21 and controller 13) does not serve as an interface to memory devices (memory BLKs 1 and 2) and does not separate them from the memory bus and system memory controller 11.

Claims 21-23 and 30-32 are rejected under 35 U.S.C. 102 (e) as being anticipated by U.S. Patent No. 5,790,447 of Laudon et al. ("Laudon"). Laudon also fails to disclose the above limitations including a memory module controller that servers as an interface between one or more memory devices of the memory module and a system memory controller and the system memory bus. Laudon fails to disclose or suggest a memory module controller that separates the one or more memory devices from the system memory controller and the memory bus, such that the memory devices and the system memory bus can operate in different operating environments, as evident by Figs. 4 and 5 of Laudon. Therefore, independent claim 21 is not anticipated by Cox or Laudon.

Similarly, independent claim 30 includes limitations similar to those referred by claim 21. Thus, for the reasons similar to those discussed above, independent claim 30 is not anticipated by Cox or Laudon. Given that claims 22-29 and 31-40 depend from one of the above independent claims, it is respectfully submitted that claims 22-29 and 31-40 are not anticipated by Cox or Laudon.

Claims 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laudon. Claims 22 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox.

Claims 24-29 and 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox in view of Leung and Nielsen. Claims 24-29 and 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laudon in view of Leung and Nielsen.

Leung relates to a resynchronization circuit for processing a stream of data read from a memory system, while Nielsen relates to a system and method for reducing power usage by multiple memory modules. It is respectfully submitted that Leung and Nielsen also fail to disclose or suggest the above limitations referred by claim 21. There is no suggestion to combine Cox and Laudon with Leung and Nielsen. It is an impermissible hindsight to combine Cox and Laudon with Leung and Nielsen, based on applicant's own disclosure. Even if they were combined, such a combination still lacks the above limitations referred by claims 21 and 30. Given that claims 22, 24-29, and 31-40 depend from independent claims 21 and 30 respectively, for at least the reasons similar to those discussed above as applied to claim 21, claims 22, 24-29, and 31-40 are patentable over the cited references.

In addition, with respect to power management features of claims 24-29 and 33-38, it is respectfully submitted that none of the cited references discloses or suggestions the limitations cited in claims 24-29 and 33-38. The Examiner contends that Leung and Nielsen disclose systems which reduce power consumption by reducing power to part or all of one or more memory modules. The Examiner further stated:

> "It would have been obvious to one of ordinary skill in the art at the time the invention was made to include power management circuitry on the memory modules of Cox to control the power consumed by the modules. The particular method of reducing the power consumed by the modules is a matter design choice and would include all of the claimed options: reduce power to individual memory devices, decouple the devices from the bus, alter the clock frequency, and disable the clock."

(8/27/2003 Office Action, page 9).

Applicant respectfully disagrees. Power management of the memory devices is an important and an integral feature of the memory designs. It is irrelevant whether the cited references disclose the ideas of power management. It is how to manage the power consumed by the memory devices that makes the corresponding product unique and better. Applicant respectfully submits that neither Leung nor Nielsen discloses or suggests reducing power consumed by the memory devices if the memory devices are not being accessed by, for example, changing the clock and its frequency, decoupling the memory devices from the system bus, or allow the memory devices to operate at different power voltages or voltage swings, etc., as referred to by claims 24-29 and 33-38. Without the memory module controller that separates (e.g., decoupling) the memory devices from the system bus and system controller, none of the cited references is able to perform the power management in a way as claimed in the present application.

In view of the foregoing, applicant respectfully submits the present application is now in condition for allowance. Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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